

Appl. No. 09/683,693
Amtd. dated January 13, 2005
Reply to Office action of October 27, 2004

REMARKS

The claims are listed in the previous section only for the
5 Examiner's convenience. No amendments are made.

Reconsideration of claim 1-8 is respectfully requested in view
of the arguments presented below. Claims 2-4 and 6-8 are dependant
and should be allowed if claims 1 and 5 are allowed.

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1. **Rejection of claims 1-8 under 35 U.S.C. 103(a) as being
unpatentable over applicant's admitted prior art in view of
Hoshino et al. US (6,804,300):**

15 The applicant argues that Hoshino's detection circuit, which is
external to a computer, serves a purpose far removed from
controlling power to a card bus controller of a computer, and
thus, the combination does not have adequate motivation.

20 It is unclear to the applicant to which of Hoshino's elements
the Examiner is likening the claimed detection circuit.
Hoshino's PCMCIA card 3 does include a switch circuit 143 and
the power stabilizer 69 does include a card insertion detector
controller 146 and a power control signal detector 144, and each
25 of these or a combination of such could be considered a detection
circuit. However, none of these form part of the computer 1, the
applicant's claims 1-8 being directed toward a computer.
Additionally, the Examiner has not indicated motivation for
providing any of these elements 143, 146, 144 as part of a computer.

30 The applicant argues that there is no motivation for this since

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Hoshino expressly teaches element 143 as part of the PCMCIA card 3, and elements 146, 144 as part of an external power source 34, which is to have its power balanced with that of the computer

5 1. Regardless, none of these elements 143, 146, 144 are suggested as suitable to turn on or turn off a card bus controller of a computer, as recited in claims 1 and 5. Rather these elements 143, 146, 144 are taught to control power to the PCMCIA card 3 so as to coordinate supply of external power with power supplied

10 by the computer 1 (see Fig.32).

Since the elements 143, 146, 144 are not taught or suggested as part of a computer, the applicant contends that the Examiner has not considered Hoshino's teaching as a whole and that the

15 motivation indicated by the Examiner is inadequate for one of ordinary skill in the art to make the combination.

In addition, according to MPEP 2143.03, to establish *prima facie* obviousness all limitations of the claims must be taught or

20 suggested by the cited prior art. Regarding the claimed limitation of the card bus controller, Hoshino's computer 1 does indeed include a card bus bridge 31 (Fig.2), however, Hoshino does not discuss this component much (col. 10 lines 52-53), and certainly does not teach or suggest that it is turned on or off

25 depending on the connection of the PCMCIA card 3, as recited in claims 1 and 5. The applicant's admitted prior art also does not teach or suggest this.

30 The applicant respectfully requests that this rejection be withdrawn.

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2. Rejection of claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Evoy (US 6,062,480):

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According to MPEP 2143.03, to establish prima facie obviousness all limitations of the claims must be taught or suggested by the cited prior art.

10 The applicant argues that the combination of applicant's admitted prior art and Evoy does not teach or suggest at least the following limitations:

in claim 1,

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"when the detection circuit detects that there is no PCMCIA card inserted into the card bus slot, the card bus controller is turned off,"

20 and in claim 5,

"turning off the card bus controller for lowering power consumption when there is no PCMCIA card inserted into the card bus slot."

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The "turning off" limitation is supported in the applicant's disclosure in paragraph [0015]:

30 "When the detection circuit 30 detects that there is no PCMCIA card inserted into the card bus slots 24, the detection circuit

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30 will generate the check signal via port 36 for informing the processor 22 that there is no PCMCIA card inserted into the card bus slots 24. The processor 22 will then turn off the card bus 5 controller 28 via the port 38 according to the check signal in order to lower power consumption."

In this argument, the applicant assumes that the Examiner likens Evoy's bus control 18 to the claimed card bus controller (since 10 the Examiner has not explicitly indicated such). The Examiner has stated that the bus controller 18 is turned on or off depending on the detection of a connection of the card 28. The applicant contends that Evoy does not teach or suggest turning off the bus controller 18.

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Referring to Evoy's Fig. 2, a bus 22, under control of the bus controller 18, is switched between active and inactive states depending on connection of a card 28. Essentially, when the card 28 is connected, the bus controller 18 makes the bus 22 inactive 20 for a short time to allow the card 28 to fully power up. To one of ordinary skill in the art, this would likely mean that the bus controller 18 would require constant power and that it should not be turned off. Regardless, Evoy does not explicitly teach turning off the bus controller 18.

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Moreover, Evoy does not suggest turning off the bus controller 18. Turning off the bus controller 18 may affect how other PCMCIA, ROM, flash ROM devices 20 are able to interact with the CPU 26. It would not be readily apparent to one of ordinary skill in the 30 art when consulting Evoy that the bus controller 18 could be

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switched off when no card 28 is connected so as to save power. Any benefit of power saving would be outweighed by a loss of proper connectivity between the CPU 26 and the other devices 20. Thus,
5 one of ordinary skill in the art lacks motivation for making the combination.

Therefore, the combination of art does not teach or suggest all limitations of claims 1 and 5. The applicant respectfully
10 requests that this rejection be withdrawn.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. The time difference between D.C. and Taiwan is 13 hours. The preferred time period for telephone conversation is 7 AM (or
25 earlier) - 11 AM, D.C. time.